108 台大資工計結

1.

a. False.
Software pipelining is a technique used to optimize loops, in a manner that parallels hardware pipelining. Classical pipeline also benefit from software pipelining or global instruction scheduling.

b. False.

2.

a. E

b. D (It exploit instruction-level parallelism.)

c. C

3.

a. Pseudo instruction 是指實際機器並不存在但組譯程式卻可以接受的指令。虛擬指令只要透過組譯程式便可將其轉譯為機器可執行的指令。Pseudo instruction 存在的好處是可以讓 programmer 可以有更多指令可使用但不需實際擴大指令集。

b. 使用 post-increment 與 pre-increment 指令處理陣列資料存取可減少指令使用讓程式碼更為精簡。高階語言架構如:
```
for(int i = 0; I < 100; i++)
    A[i] = 0;
```
便可從 post-increment 或 pre-increment 指令的使用得到好處。

c. Post-increment 與 pre-increment 指令功能類似且無互補功能，因此只要存在一種即可。

d. 指令集包含像是 post-increment load 這種較複雜的指令會讓計算機規格變複雜，在實作機器時會增加困難度且降低效能。

4.

a. User-defined interrupt(instruction) allow program running in user mode to request privileged operations that are in Supervisor mode.

Exception	Page fault, TLB miss, Floating point arithmetic underflow, Undefined instruction, User defined interrupt, Execution abort, System call
Interrupt	I/O device request

b.

Rank	1	2	3	4	5	6
Micro-architectures	Superscalar implementation	Speculative execution	Out-of-order superscalar	Pipelined implementation	Single issue In-order processor	Hierarchical data caches

c. A container is a standard unit of software that are packages up code and all its dependencies so the application runs quickly and reliably from once computing environment to another.

Rank	1	2	3	4	5	6
Processor	GPGPU	Containers	Virtual Machines	Hyper-threaded processor	Superscalar processor	Pipelined processor

5.

a.

Acronyms	Meaning
ILP	Instruction-level parallelism is a measure of how many of the instructions in a computer program can be executed simultaneously.
DLP	Data-level parallelism is the parallelism achieved by operating on independent data.
MLP	Memory-level parallelism refers to the ability to have pending multiple memory operations, in particular cache misses or translation lookaside buffer (TLB) misses, at the same time.
TLP	Thread-level parallelism is the parallelism inherent in an application that runs multiple threads at once.

b.

Acronyms	Architecture/ Microarchitecture
ILP	Pipelined processor
DLP	SIMD
MLP	Superscalar with non-blocking cache
TLP	Hyper-threaded processor

c.

Acronyms	Software technique
ILP	Loop unrolling and register renaming by compiler
DLP	Loop-level optimization technique by compiler
MLP	Software pipelining, a type of out-of-order execution, is done by a compiler
TLP	Loop-level parallelism in software programming

6.

a. Reject.

b. 不同 cluster 的 core 只能以網路連接，因此屬於 NUMA 架構，故可以使用 Directory 協定維持不同 cache 間資料的一致性